

REMARKS/ARGUMENTS

Claims 1-15 stand rejected in the fifth and non-final Official Action. No claim amendments are offered, but newly written claims 16-29 are offered for consideration. Accordingly, claims 1-29 remain in this application.

The Examiner rejects Applicants' independent claims and claims dependent thereon upon yet another new and not previously before cited reference by itself or in combination with other references. Applicants note that this Official Action is the fifth Official Action in this application, four of which have been non-final. This applicant, therefore, respectfully requests that this application be transferred to another examiner in the art unit for final resolution. Applicants will also make a formal request to the Group Director in order to expedite not only the transfer, but to obtain either an allowance or a valid action on the merits of the above claims.

Looking at the newest rejection of the claims, the Examiner alleges that claims 1, 4, 5 and 11-15 are anticipated under 35 USC §102 by Tailliet (U.S. Patent 6,848,049). Applicants' claims specify a method of "modifying the content of the non-volatile memory of a contactless microcircuit card." (emphasis added). The Examiner alleges that Tailliet discloses "a method of modifying the content of the non-volatile memory of a microcircuit card" and references column 3, lines 20-25 of Tailliet as allegedly teaching such disclosure (see the Official Action, page 2, section 5). However, the cited portion of the Tailliet reference, and, indeed, the entire Tailliet reference, fails to contain any disclosure of a method of modifying the content of the memory of a microcircuit card.

Instead, the Examiner's cited portion of Tailliet only refers to modification of the response time ("it may be a modification of a response time with respect to a particular

instruction, a response time with respect to an exchanged data element or the like." Tailliet, column 3, lines 22-25). Again, because the Examiner can cite no disclosure of Applicants' claimed structure or claimed method steps, any further rejection of claims 1, 4, 5 and 11-15 as being anticipated by Tailliet clearly fails.

Applicants note that independent claim 1 recites steps a) and b). Step a) requires "modifying the contents of the card memory by provisionally recording in the card memory each of said interdependent items of information without losing prior values corresponding to said items." The Examiner alleges that this method step is disclosed in Tailliet at column 4, lines 39-59. However, the cited portion of the Tailliet reference merely discusses a detection means and its operation in consequence to various registers. The cited portion discloses two different possible scenarios, but neither appears to have anything to do with Applicants' claimed modifying the contents of a card memory by provisional recording.

The Examiner also alleges that step b) of Applicants' independent claim 1 is disclosed in Tailliet between column 5, line 50 and column 6, line 10. Again, the cited portion of Tailliet appears to have nothing to do with step b) of claim 1, i.e., finalizing the modifications to the card memory by one of (a) confirming all of the modifications and by (b) discarding all of the modifications.

With reference to the Examiner's discussions on page 3 of the Official Action with respect to steps a) and b), while he appears to accurately quote those steps, the cited portions of the Tailliet reference appear to have nothing to do with either step, let alone Applicants' claimed method of modifying the content of the memory of a contactless microcircuit card. As in previous responses by Applicant, should the Examiner believe that claimed structure and method

steps are present in the Tailliet reference, he is respectfully requested to identify the location of such teaching.

Nowhere else in the Official Action does the Examiner provide any further clue as to how he believes the Tailliet reference contains any disclosure of Applicants' claimed invention. Accordingly, any further rejection of claim 1 or claims dependent thereon based upon the Tailliet reference either by itself or in combination with other references is respectfully traversed.

Claims 2 and 3 stand rejected under 35 USC §103 as unpatentable over Tailliet in view of Fujisaki (U.S. Patent 4,877,945). Because claims 2 & 3 depend from claim 1, the above comments distinguishing claim 1 from the Tailliet reference is incorporated by reference.

The Examiner's multiple admissions as to the deficiencies of the Tailliet reference teaching with respect to the limitations of claims 2 & 3 in the paragraph bridging pages 4 and 5 of the Official Action are very much appreciated. However, the Examiner does not allege that the secondary reference, Fujisaki, teaches the above-noted aspects of Applicants' independent claim 1, i.e., a method of modifying the content of a memory of a card or the two specific steps recited in claim 1. While the Examiner alleges that Fujisaki discloses the admittedly missing aspects of claims 2 and 3, the Examiner merely makes a reference to Fujisaki's column 2, lines 10-56 without indicating how or where he believes it contains the missing disclosures. It is to be remembered that the burden is on the Examiner to establish where claimed structures exist in a prior art reference in order to make out a *prima facie* case for unpatentability.

Moreover, the Examiner fails to provide any reason or motivation for combining the Tailliet and Fujisaki references in accordance with his burden of establishing a *prima facie* basis of unpatentability under §103. Additionally, the Examiner appears to ignore the Tailliet teaching

that one should modify the "response," i.e., the response time with respect to a particular instruction (see Tailliet, column 3, lines 23-25) instead of modifying the content of a card memory as required by the claims. Thus, Tailliet would actually lead one of ordinary skill in the art away from Applicants' claimed combination, further confirming the non-obviousness of claim 1 and claims 2 and 3 dependent thereon.

Claims 7 and 9 stand rejected under 35 USC §103 as unpatentable over Tailliet in view of Ohashi (U.S. Patent 5,761,309). Because claims 7 & 9 depend ultimately from claim 1, the above comments distinguishing claim 1 from the Tailliet reference is incorporated by reference.

Again, the Examiner's multiple admissions of what is not taught in the Tailliet reference in the first paragraph under section 7, page 6 of the Official Action are very much appreciated. As noted above, however, the Examiner fails to point out how or where the secondary reference, Ohashi, teaches any method for modifying the memory content of a microcircuit card or in particular one with the steps of a) and b) noted with respect to claim 1. Inasmuch as claims 7 and 9 ultimately depend from claim 1, it is clear that neither reference, Tailliet nor Ohashi, contain a teaching of the claimed aspects of these claims and thus there is no *prima facie* basis of unpatentability.

As above, the Examiner fails to provide any "reason" or "motivation" for combining the Tailliet and Ohashi references. Additionally, the Examiner ignores the fact that Tailliet appears to lead one of ordinary skill in the art away from the claimed combination. Clearly, the Examiner has failed to establish any *prima facie* case of obviousness under 35 USC §103 and any further rejection of claims 7 and 9 are respectfully traversed.

Claims 6, 8 and 10 stand rejected under 35 USC 103 as unpatentable over Tailliet in view of Vanstone (U.S. Patent 6,178,507). Because claims 6, 8 & 10 depend at least indirectly from claim 1, the above comments distinguishing claim 1 from the Tailliet reference is incorporated by reference.

As before, Applicants very much appreciate the Examiner's multiple admissions as to Tailliet failing to teach or suggest features of claims 6, 8 and 10 (the Official Action, page 7, section 8, first paragraph). While the Examiner alleges that the secondary reference, Vanstone, teaches "mutual authentication between a terminal and a smart card using certificates," there is no allegation that Vanstone teaches the admittedly missing elements of the Tailliet reference. Thus, even if Tailliet and Vanstone were combined, the Examiner admits that the limitations of claims 6, 8 and 10 are not taught.

Moreover, the Examiner merely provides a conclusory statement that it would be obvious to combine Tailliet and Vanstone, but fails to provide any "reason" or "motivation" for such combination. Additionally, the Examiner ignores the fact that claims 6, 8 and 10 all depend ultimately from claim 1 and the above comments with respect to claim 1 distinguishing over Tailliet are herein incorporated by reference. Further, the Examiner does not apparently appreciate that Tailliet's teaching of modifying response time would lead one of ordinary skill in the art away from Applicants' claimed method of modifying the content of a microcircuit card memory. Accordingly, any further rejection of dependent claims 6, 8 and 10 over the Tailliet and Vanstone combination is respectfully traversed.

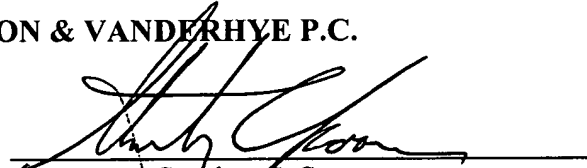
Applicants offer for consideration newly written claims 16-29 which correspond to claims already allowed in the European Patent Office and requests consideration of these newly submitted claims.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that claims 1-29 are in condition for allowance and notice to that effect is respectfully solicited. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, he is respectfully requested to contact Applicants' undersigned representative.

Respectfully submitted,

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